Ref:
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Applicant: Hui Peng
Art Unit: 2811
Application Title: Texture on Substrate and a Method for Localizing and Minimizing Effects of Lattice Mismatch
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Claims:

What I claim are:

1. A semiconductor device, comprising

   a substrate with texture on one of its two surfaces, and

   an epitaxial layer comprising an active layer and grown on the top of said texture.
2. The semiconductor device of claim 1, further comprising buffer layer grown in between said epitaxial layer and said texture.
3. The semiconductor device of claim 1, wherein said texture comprising wells and walls.
4. The semiconductor device of claim 3, wherein the width of said walls is in a range of nanometers to micrometers.
5. The semiconductor device of claim 3, wherein the depth of said well is in a range of nanometers to micrometers.
6. The semiconductor device of claim 3, wherein said wells have the shape of said semiconductor device.
7. The semiconductor device of claim 6, wherein the dimension of said wells is in the range of nanometers to micrometers.
8. The semiconductor device of claim 1, wherein said substrate emits light.
9. The semiconductor device of claim 1, further comprises a second texture formed on the top of said epitaxial layer.
10. The semiconductor device of claim 9, further comprises a second epitaxial layer grown on the top of said second texture and comprising a second active layer.
11. The semiconductor device of claim 10, further comprising a second buffer layer grown in between said second epitaxial layer and said second texture.

PCT Form 210 (PCT/JP01/01178).
PCT Form 210 (PCT/JP01/01663).
PCT Form 210 (PCT/JP00/09121).
PCT Form 210 (PCT/JP00/09220).
PCT Forms 338 and 409 (IPER) (PCT/JP01/02695) and translations.
PCT Forms 338 and 409 (IPER) (PCT/JP01/01663) and translations.
PCT Forms 338 and 409 (IPER) (PCT/JP00/09120) and translations.
PCT Forms 338 and 409 (IPER) (PCT/JP01/01928) and translations thereof.
PCT Forms 338 and 409 (IPER) (PCT/JP01/01396) and translations thereof.
European Search Report (EP 27279) Feb. 15, 2002.
PCT Forms 338 and 409 (IPER) (PCT/JP00/09121) and translations.
Wolf et al., "Silicon Processing for the VLSI Era," vol. 1, p. 5, Lattice Press, 1986.

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## *Claims*

What is claimed is:

1. A method for manufacturing a group III nitride compound semiconductor, which hardly grows epitaxially on a substrate by crystal growth, comprising:

forming a buffer layer on said substrate into an island pattern such as a dot pattern, a striped pattern, or a grid pattern such that substrate-exposed portions are formed in a scattered manner; and

forming a group III nitride compound semiconductor layer on said island patterned buffer layer by growing said group III nitride compound epitaxially in longitudinal and lateral directions; wherein a width of said substrate-exposed portions fall within the range of 1 to 10 multiplied by a width of said island patterned buffer layer.

2. A method for manufacturing a group III nitride compound semiconductor according to claim 1, further comprising:

combining epitaxial growth of said group III nitride compound formed on said island patterned buffer layer in a longitudinal direction and epitaxial growth of said group III nitride compound in a lateral direction by using the difference between the velocities of epitaxial growth of said group III nitride compound semiconductor layer on said buffer layer and on said substrate, in order to obtain a group III nitride compound semiconductor layer which covers the surface of said substrate.

3. A method for manufacturing a group III nitride compound semiconductor according to claim 1, wherein said substrate is made of sapphire.

4. A method for manufacturing a group III nitride compound semiconductor according to claim 1, wherein said buffer layer is made of aluminum nitride (AlN).

5. A method for manufacturing a group III nitride compound semiconductor according to claim 1, wherein said group III nitride compound semiconductor growing in a lateral direction does not comprise aluminum (Al).

6. A method for manufacturing a group III nitride compound semiconductor according to claim 1, further comprising:

forming an another group III nitride compound semiconductor layer on said group III nitride compound semiconductor in order to obtain a light-emitting group III nitride compound semiconductor device, wherein said group III nitride compound semiconductor is formed on a region where said island patterned buffer layer is not formed.

7. A method for manufacturing a group III nitride compound semiconductor according to claim 1, further comprising:

removing said substrate in order to obtain only said group III nitride compound semiconductor layer.

8. A light-emitting group III nitride compound semiconductor device formed by the method of claim 6.

9. A group III nitride compound semiconductor substrate formed by the method of claim 7.

***Description***

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a group III nitride compound semiconductor. Especially, the present invention relates to a method for manufacturing a group III nitride compound semiconductor in which an epitaxial lateral overgrowth (ELO) method is used to form a layer on a substrate. The present invention also relates to a light-emitting device using a group III nitride compound semiconductor formed on a group III nitride compound semiconductor layer using the ELO method. A group III nitride compound semiconductor can be made of binary compounds such as AlN, GaN or InN, ternary compounds such as Al.sub.x Ga.sub.1-x N, Al.sub.x In.sub.1-x N or Ga.sub.x In.sub.1-x-y N (0<x<1), or quaternary compounds Al.sub.x Ga.sub.y In.sub.1-x-y N (0<x<1, 0<y<1, 0<x+y<1), that is, those are represented by a general formula Al.sub.x Ga.sub.y In.sub.1-x-y N (0.ltoreq.x.ltoreq.1, 0.ltoreq.y.ltoreq.1, 0.ltoreq.x+y.ltoreq.1).

2. Description of the Related Art

A group III nitride compound semiconductor is a direct-transition-type semiconductor having a wide emission spectrum range from ultraviolet to red, and is applied to light-emitting devices such as light-emitting diodes (LEDs) and laser diodes (LDs). The group III nitride compound semiconductor